1. **What is Moore’s Law? Why and how was it modified in 1975?**

Moore’s law predicted that the number of transistors integrated on a die would grow exponentially i.e. doubling every 12 to 18 months, though the cost of the computers would be halved.

After 1975, the slope of the graph decreased. Thus, the transistors would double approximately every two years rather than 1 year or 18 months. [Graph from slide].

1. **What is the impact of Moore’s law on the development of VLSI?**
2. **Explain the brief history of IC industry.**
3. **Explain the different steps in VLSI realization process.**

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1. **What are the problems of VLSI design on today?**

* Verification of correctness-logic and timing.
* Ensuring reliable operation
* Testing

1. **How do you define LSI and VLSI?**

**LSI-** Large scale integration (105 components per chip)

**VLSI-**Very Large Scale Integration (105 – 106 components per chip)

1. **What is yield? How cost is related to yield in chip designing?**

Fraction (or percentage) of good chips produced in a manufacturing process is known as yield (Y).

1. **What is verification?**

Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.

1. **Explain VLSI design Cycle.**

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1. **What is semiconductor?**

Semiconductors are materials which have a conductivity between conductors and nonconductors or insulators. Semiconductors are made from pure elements, typically silicon or geranium, or compounds such as gallium arsenide.

1. **Explain the Energy Band theory of crystal.**
2. **In the light of energy band theory, explain semiconductor, metal, insulator.**

The diagram of conduction band, forbidden gap and valence band.

1. **Why Si, Ge are semiconductors?**
2. **What are holes? Explain how holes can be carrier of electricity.**
3. **What is doping in semiconductor? What are its effects?**

* Increases conductivity
* Produces conductors in which electric carriers are either predominantly holes or predominantly electrons
* In n-type semiconductor, majority carrier is electrons and carrier is holes
* In p-type semiconductor, majority carrier is holes and minority carrier is electrons

1. **Explain donor and acceptor impurity in semiconductors?**
2. **What is semiconductor diode? What is depletion region? Explain the operation of semiconductor diode with both forward and reverse biased.**
3. **Explain Bipolar junction transistor.**
4. **Explain its three modes of operation of a bipolar transistor.**
5. **How does bipolar transistor act as an amplifier?**
6. **How does transistor act as a switch?**
7. **Compare the operations of semiconductor diode and transistor.**
8. **What are the problems of bipolar junction transistor?**

* Power density increased
* Device variability
* Reliability
* Complexity
* Leakage
* Power dissipation limits device density
* Transistor will operate near ultimate limits of size and quality– eventually, no transistor can be fundamentally better

1. **Classify Field effect transistors.**
2. **Sketch the basic structure of an n-channel field effect transistor.**
3. **Explain the characteristics of JFET. How does it behave for small VDS and large VDS? How and when it turns from ohomic region to saturation region?**
4. **Define pinch-off voltage. Sketch the depletion region before and after pinch-off.**
5. **Explain JFET as amplifier and switch.**
6. **Compare bipolar junction transistor versus junction field effect transistor**
7. **Explain MOSFET. What are the advantages of MOSFET over JFET?**
8. **Explain MOSFET with both enhancement and depletion mode.**
9. **Explain how MOSFET act as a switch.**
10. **Compare p channel and n channel MOSFET**
11. **Classify different Field Effect transistors.**
12. **Compare the transfer characteristics in JFET, depletion type MOSFET, enhancement type MOSFET.**
13. **Compare Silicon versus Germanium in the use of chip designing.**
14. **Explain the functioning of nMOS inverter considering the load as a) resistor b) enhancement type transistor c) depletion type transistor.**
15. **What is the problem of the nMOS inverter with pull up as an enhancement type? How is it improved with depletion type pull up?**
16. **What are the drawbacks of MOSFETs?**
17. **What are the advantages of CMOS over MOSFET? What are the disadvantages of CMOS design?**
18. **How does CMOS work as an inverter?**
19. **Implement the Boolean function *f=* *ab*+ + *abd+*+ *acd* with the help of nMOS.**
20. **Implement the Boolean function *f=* *ab*+ + *abd+*+ *acd* with the help of pMOS.**
21. **Implement the Boolean function *f=* *ab*+ + *abd+*+ *acd* with the help of a) CMOS Nand CMOS Nor.**
22. **What is single complex cell design in CMOS? What are its advantages and disadvantages of it?**
23. **Implement the Boolean function *f=* *ab+*+ *abd +*+ *acd* using single complex cell designs in four different ways (consider that for any input, its complement is also available).**
24. **How are the circuits optimized at different levels?**
25. **What is the significance of stick diagram, as applicable in the design of VLSI?  What is its advantage and limitation?**
26. **Draw the layout of NAND and NOR using CMOS designs.**
27. **How to reach mask diagram from stick diagram.**
28. **Draw the coloured stick and mask diagrams for implementing the following Boolean functions :**

**i)                     f =  A`B  + Ā`C [ using n MOS transistors]**

**ii)                   g = ( w +x + z). (`w  + xz )  [ using C MOS transistors ]**

1. **Draw the coloured stick and mask diagrams for implementing the following Boolean functions : (i) f = W `XZ + `W`Y  [ using n MOS transistors]**

**(ii) g = (A + `B + D) (`A + BD) [using CMOS transistors ]**

1. **Draw the coloured stick and mask diagrams for implementing the following Boolean functions : (i) f = A`B + `AC +`CD  [ using n MOS transistors]**

**(ii) g = (w + `x ) (`y + z) [using CMOS transistors ]**

1. **Draw the coloured stick and mask diagrams for implementing the following Boolean functions : (i) f = (w+`x +`z) (`w+y+x)  [ using n MOS transistors]**

**(ii) g =  `AC`D + A`BC [using CMOS transistors ]**

1. **Draw the coloured stick and mask diagrams for implementing the following Boolean functions : (i) f = A`BC + `AB`C  [ using n MOS transistors]**

**(ii) g = (`w +x+z) (w+`x +`z) [using CMOS transistors ]**

1. **Draw the stick diagram of a shift register cell using a transmission gate followed by a CMOS inverter.**
2. **Convert the stick diagram obtained in previous question to symbolic form and show an example of optimization in it.**
3. **Discuss the problems of manufacturing in sizing of the different elements in fabrication.**
4. **What is design rule? What is the advantage of generalized design rule?**
5. **What do you mean by l–based IC design rules?**
6. **What are the rules of design rules?**
7. **Explain nMOS design rules.**
8. **Explain buring contact and butting contact in nMOS design. Compare their merits and demerits.**
9. **Explain CMOS design rules.**
10. **Explain the design rules for different contact cuts.**
11. **Explain the design rules for via and cut.**
12. **For a CMOS shift register cell (as in question 56 and 57) draw the mask diagram conforming the l–based design rules.**
13. **Compare silicon versus Germanium in fabrication.**

Initially, Ge was used for fabrication, but later Si took over.

* Large variety of process steps possible without problem of decomposition
* Si has a higher band gap than Ge and also higher operating temperature.
* Si readily forms native oxide.
  + High quality insulator
  + Protects and passivates underlying circuitry
  + Helps in patterning
  + Useful for dopant masking
* Si is cheap and abundant.

Si disadvantages

* Low carrier mobility
* Weak adsorption and emission of light
* Most opto electronic applications not possible.

1. **Why is silicon preferred for fabrication?**
2. **How the silicon wafer is prepared from sand? Explain the steps.**
3. **What is photoresist? Explain its uses in fabrication process.**

A light-sensitive, acid-resistant organic polymer. If the UV light strikes the photoresist (which is initially insoluble), becomes soluble in certain solutes.

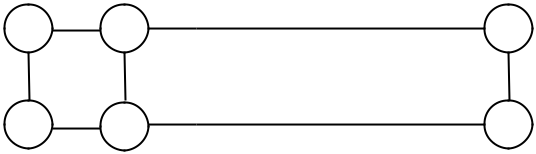
Use:

* **Delineation for Etching**. A blanket deposition is made on the wafer, then photoresist patterning covers the areas to be SAVED. After developing, the wafer is etched and all parts NOT COVERED by photoresist are removed.
* **Delineation for Deposition**. For ion implantation, areas are opened for doping the silicon. The photoresist absorbs all ions except for the areas which are open. In these areas (e.g. Drain or Source wells) the ions penetrate into the silicon.

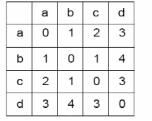
1. **Define lithography.**

In general, a layer must be patterned before the next layer of material is applied on chip. The process used to transfer a pattern to a layer on the chip is called lithography.

1. **Explain the basic processing steps in fabrication.**
2. **Describe etching process.**
3. **What is the role of silicon dioxide in fabrication?**
4. **Explain the different steps in nMOS fabrication.**
5. **What is polysilicon? What is its use in fabrication process?**
6. **Explain the chemical vapour deposition technique.**
7. **Explain the different fabrication steps in CMOS. Compare the p-well and n-well process in CMOS fabrication.**
8. **What is partitioning? Why do we need it?**
9. **What are the different levels of partitioning?**
10. **Consider a hypergraph H, where each hyperedge interconnects at most three vertices. We model each hyperedge of degree-3 with three edges of weight ½, on the same set of vertices, to obtain a weighted graph G. Prove that an optimal balanced partitioning of G corresponds to an optimal balanced partitioning of H.**
11. **In refer to Question 3, prove that optimal balanced partitioning of G cannot be done if each edge of H interconnects at most four vertices (i.e., give a counter example).**
12. **Explain Kernighan-Lin algorithm for partitioning a graph. Find its time complexity.**
13. **Consider a path graph v1, v2,….., vn. That is, v1 is connected to vi+1, for 1 < i < n-1. Apply the Kernighan-Lin algorithm to this graph. As the initial partition, let va, for all odd values of a be in one set , and vb, for all even values of b, be in the other set.**
14. **Consider a complete binary tree with n nodes. Apply Kernighan-Lin algorithm to this graph. As the initial partition, let va, for all internal vertices, be in one set and vb, for all leaves, be in the other set.**
15. **Show how the Kernighan-Lin Heuristic works on the ladder graph with 2n vertices, starting with initial partition of V1= {1,2,3,……,n}, and V2={n+1,n+2,n+3,…..,2n}.**

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1. **What are the drawbacks of Kernighan-Lin algorithm?**
2. **The following matrix provides 4 modules a,b,c,d with their entries representing the number of connections between the two modules. Apply Kernighan-Lin heuristic to obtain the partitioning.**

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1. **What are the advantages of Fiduccia-Mattheyses algorithm over Kernighan-Lin algorithm?**
2. **What are the similarities between Fiduccia-Mattheyses algorithm and Kernighan-Lin algorithm?**
3. **Present the Fiduccia-Mattheyses Algorithm. Find out its time complexity.**
4. **Apply Fiduccia-Mattheyses Algorithm for the problem in question 7.**
5. **Apply Fiduccia-Mattheyses Algorithm for the problem in question 8.**
6. **Apply Fiduccia-Mattheyses Algorithm for the problem in question 10.**
7. **“There is a trade off associated for partitioning with replication.” Is it true or false? Justify.**
8. **Discuss how Partitioning is affecting overall delay.**
9. **What do you understand by performance driven partitioning?**
10. **Discuss the approach of clustering in case of partitioning.**
11. **Define Floor planning. Define sliceable and non-sliceable floorplan with examples. What are the advantages of sliceable floorplan?**
12. **State with an example how a sliceable floorplan can be represented by a binary tree.**
13. **When an adjacency graph cannot admit a rectangular dual?**
14. **Obtain the hierarchical floorplan tree for the floorplan given in Fig.5.**
15. **Illustrate the steps of rectangular dualization on an inherently non-sliceable graph of n vertices.**
16. **Obtain a rectangular dual of the following adjacency graph.**

**Fig. 3**

1. **Obtain the rectangular dual of the following adjacency graph below of Fig. 4.**
2. **Are the Floorplans obtained in 17 and 18 sliceable?**
3. **Prove that there is a one-to-one correspondence between a sliceable floorplan and a normalized Polish expression.**
4. **Give the adjacency graph for the following floorplan of Fig.5.**

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| --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | | | 3 | | 4 |
| 13 | 17 | | | 14 |
| 12 | | 5 | |
| 11 | | 6 | |
| 10 | 16 | 15 | 7 |
| 9 | | 8 | | |

**Fig. 4 Fig.5**